

**TITLE**

**DYNAMIC RANDOM ACCESS MEMORY CELL LAYOUT AND FABRICATION**  
**METHOD THEREOF**

**BACKGROUND OF THE INVENTION**

**5 Field of the Invention**

The invention relates to a memory cell of a semiconductor device, and more particularly to a dynamic random access memory (DRAM) cell layout for arranging deep trenches and active areas and a fabrication method thereof.

**10 Description of the Related Art:**

A dynamic random access memory (DRAM) cell typically includes a memory cell coupled to a storage capacitor. Generally the storage capacitor is formed within a deep trench etched into a semiconductor substrate. The storage  
15 capacitor is accessed using an access transistor which allows charge to be stored in the storage capacitor or retrieves charge from the storage capacitor depending on whether the desired action is a read or write function. For a buried strap type trench capacitor, dopant outdiffusion  
20 near a wordline can cause a short channel effect in the access transistor channel, thus reducing subthreshold conduction and causing a fail in retention time.

FIG. 1 is a conventional DRAM cell layout. Deep trench capacitors 10 are disposed under passing wordlines 12.  
25 Access transistors 14 are electrically coupled to storage nodes 16 of the trench capacitors 10 through diffusion regions 18 which may be either a source or a drain of the

access transistors 14. Diffusion regions 20 are electrically connected to bitline contacts 22 which connect to bitlines (not shown) to read and write to the storage nodes 16 through the access transistors 14. Access  
5 transistors 14 are activated by the wordlines 12. When voltage is applied to the wordlines 12, a channel below the wordline 12 conducts and allows current to flow between diffusion regions 18 and 20 and into or out of the storage node 16. Wordlines 12 are preferably spaced across the  
10 smallest possible distance to conserve the layout area. The smallest possible distance is typically a minimum feature size "F".

FIG. 2 is a cross-section along line 2-2 of FIG. 1. Elements of FIG. 2 are labeled as described in FIG. 1. The  
15 storage nodes 16 are isolated from a doped well 24 by a dielectric collar 26. A shallow trench isolation (STI) 28 is provided over the storage nodes 16 to electrically isolate the passing wordlines 12 formed above storage nodes 16. The diffusion region 18 of the access transistor 14 is  
20 connected to the storage node 16 through a buried strap (BS) 32 and a BS out-diffusion region 30. Considering an overlay tolerance effect, a BS merge phenomenon easily occurs to cause a short channel effect in a channel region 34 underlying a gate electrode 36 of the access transistor 14.

## 25 SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a DRAM cell layout and a fabrication method thereof to improve subthreshold conduction and retention time performance.

Client's ref. :91234  
Our ref: 0548-10164-us/final/Cherry/Steve

According to the object of the invention, a dynamic random access memory cell layout has a first gate conductor pair and a second gate conductor pair extending along a first direction, in which each gate conductor pair comprises  
5 a first gate conductive line and a second gate conductive line. A bitline pair has a first bitline and a second bitline, which extend along a second direction and intersect the gate conductor pairs. Corresponding to the first bitline, a first active area extends along the second  
10 direction to cross the first gate conductor pair. Corresponding to the second bitline, a second active area extends along the second direction to cross the second gate conductor pair. Each active area has a first deep trench and a second deep trench formed in a substrate underneath  
15 the first gate conductive line and the second gate conductive line, respectively. A bitline contact is formed between the first gate conductive line and the second gate conductive line to be electrically connected to the corresponding bitline. A common source/drain region is  
20 formed in the substrate between the first gate conductive line and the second gate conductive line to be electrically connected to the bitline contact. A first vertical transistor and a second vertical transistor are formed overlying the first deep trench and the second deep trench,  
25 respectively. Each vertical transistor has a buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the deep trench.

## DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 is a conventional DRAM cell layout.

FIG. 2 is a cross-section along line 2-2 of FIG. 1.

FIG. 3 is a DRAM cell layout of deep trenches and active areas according to the first embodiment of the present invention.

FIG. 4 is a cross-section along line 4-4 of FIG. 3.

FIG. 5 is a DRAM cell layout of deep trenches and active areas according to the second embodiment of the present invention.

FIG. 6 is a three-dimensional diagram of a vertical transistor according to the second embodiment of the present invention.

FIGS. 7A~7L are cross-sections of a fabrication method for above-described deep trenches and vertical transistors.

## DETAILED DESCRIPTION OF THE INVENTION

### First Embodiment

FIG. 3 is a DRAM cell layout of deep trenches and active areas according to the first embodiment of the present invention. The DRAM cell layout comprises a plurality of gate conductor pairs  $P_1$ ,  $P_2$  and  $P_3$  and a plurality of bitlines  $BL_1$  and  $BL_2$ . Each of the gate

conductor pairs  $P_1$ ,  $P_2$  and  $P_3$  comprises a first gate conductive line  $GC_1$  and a second gate conductive line  $GC_2$  arranged parallel to each other. The gate conductive lines  $GC_1$  and  $GC_2$  extending along a first direction and the  
5 bitlines  $BL_1$  and  $BL_2$  extending along a second direction intersect to define a plurality of DRAM cells. A first active area  $AA_1$  is defined at the intersection of the second gate conductor pair  $P_2$  and the first bitline  $BL_1$ . A second active area  $AA_2$  is defined at the intersection of the first  
10 gate conductor pair  $P_1$  and the second bitline  $BL_2$ , alternatively, at the intersection of the third gate conductor pair  $P_3$  and the second bitline  $BL_2$ .

The first active area  $AA_1$  extends along the first bitline  $BL_1$  to cross the first gate conductive line  $GC_1$  and  
15 a second gate conductive line  $GC_2$  of the second gate conductor pair  $P_2$ , and comprises two vertical transistors  $T_1$  and  $T_2$ , a common bitline contact BC and two deep trenches  $DT_1$  and  $DT_2$ . The first vertical transistor  $T_1$  is formed on a region where the first deep trench  $DT_1$  is partially  
20 overlapped with the first gate conductive line  $GC_1$ . The second vertical transistor  $T_2$  is formed on a region where the second deep trench  $DT_2$  is partially overlapped with the second gate conductive line  $GC_2$ .

The second active area  $AA_2$  extends along the second  
25 bitline  $BL_2$  to cross the first gate conductive line  $GC_1$  and a second gate conductive line  $GC_2$  of the first gate conductor pair  $P_1$ . Alternatively, the second active area  $AA_2$  crosses the first gate conductive line  $GC_1$  and a second gate conductive line  $GC_2$  of the third gate conductor pair  $P_3$ .  
30 The second active area  $AA_2$  comprises two vertical

transistors  $T_1$  and  $T_2$ , a common bitline contact BC and two deep trenches  $DT_1$  and  $DT_2$ . The first vertical transistor  $T_1$  is formed on a region where the first deep trench  $DT_1$  is partially overlapped with the first gate conductive line  $GC_1$ . The second vertical transistor  $T_2$  is formed on a region where the second deep trench  $DT_2$  is partially overlapped with the second gate conductive line  $GC_2$ .

FIG. 4 is a cross-section along line 4-4 of FIG. 3. For the first active area  $AA_1$ , the first deep trench  $DT_1$  and the second deep trench  $DT_2$  are formed by etching a semiconductor silicon substrate 40, and a shallow trench isolation structure STI is formed outside the first deep trench  $DT_1$  and the second deep trench  $DT_2$  for isolating the first active area  $AA_1$  from the second active area  $AA_2$ . A first deep trench capacitor  $C_1$  and a second deep trench capacitor  $C_2$  are formed at the lower portions of the first deep trench  $DT_1$  and the second deep trench  $DT_2$ , respectively. A first buried strap out-diffusion region  $BS_1$  is formed in the substrate 40 adjacent to one sidewall of the middle portion of the first deep trench  $D_1$ . The first buried strap out-diffusion region  $BS_1$  serves as a source/drain region of the first vertical transistor  $T_1$ , and provides an electrical connection between the first vertical transistor  $T_1$  and the first deep trench capacitor  $C_1$ . Similarly, a second buried strap out-diffusion region  $BS_2$  is formed in the substrate 40 adjacent to one sidewall of the middle portion of the second deep trench  $D_2$ . The second buried strap out-diffusion region  $BS_2$  serves as a source/drain region of the second vertical transistor  $T_2$ , and provides an electrical connection between the second

vertical transistor  $T_2$  and the second deep trench capacitor  $C_2$ . The first gate conductive line  $GC_1$  partially overlaps the upper portion of first deep trench  $DT_1$  to serve as a gate electrode of the first vertical transistor  $T_1$ . The  
5 second gate conductive line  $GC_2$  partially overlaps the upper portion of second deep trench  $DT_2$  to serve as a gate electrode of the second vertical transistor  $T_2$ . A common source/drain region S/D is formed in the substrate 40 between the first gate conductive line  $GC_1$  and the second  
10 gate conductive line  $GC_2$ . Thus, a first vertical channel region is provided between the common source/drain region S/D and the first buried strap out-diffusion region  $BS_1$ , and a second vertical channel region is provided between the common source/drain region S/D and the second buried strap  
15 out-diffusion region  $BS_2$ . The bitline contact BC is formed overlying the common source/drain region S/D and electrically connected to the first bitline  $BL_1$ . Accordingly, the DRAM cell layout of the vertical transistors  $T_1$  and  $T_2$  and the deep trenches  $DT_1$  and  $DT_2$  can  
20 prevent deterioration of subthreshold conduction, thus improving retention time performance.

### **Second Embodiment**

FIG. 5 is a DRAM cell layout of deep trenches and active areas according to the second embodiment of the  
25 present invention. FIG. 6 is a three-dimensional diagram of a vertical transistor according to the second embodiment of the present invention. Elements similar to those shown in FIGS. 3 and 4 are omitted here.

The DRAM cell layout of deep trenches and active areas  
30 of the second embodiment is substantially similar to that of

the first embodiment, with the similar portions omitted herein. The different portion is the profile of the overlapping region between the deep trench and the vertical transistor. In the first embodiment, on the overlapping  
5 region between the deep trench and the vertical transistor, the sidewall profile of the deep trench is a line. Comparatively, in the second embodiment, on the overlapping region between the deep trench and the vertical transistor, the sidewall profile of the deep trench comprises at least  
10 three edges. For example, a five-edge sidewall profile, such as a  $\square$ -shaped sidewall.

Preferably, on an active area AA, the first deep trench DT<sub>1</sub> is partially overlapped with the first gate conductive line GC<sub>1</sub>, and the first deep trench DT<sub>1</sub> comprises a  $\square$ -shaped  
15 sidewall within the overlapping portion therebetween. Similarly, the second deep trench DT<sub>2</sub> is partially overlapped with the second gate conductive line GC<sub>2</sub>, and the second deep trench DT<sub>2</sub> comprises a  $\square$ -shaped sidewall within the overlapping portion therebetween. Therefore, the  
20 vertical channel region between the common source/drain region S/D and the buried strap out-diffusion region BS becomes a multilateral structure, viewed as a three-dimensional design, which can further improve subthreshold conduction and retention time performance.

### 25 Third Embodiment

FIGS. 7A~7L are cross-sections of a fabrication method for above-described deep trenches and vertical transistors.

In FIG. 7A, an array area I and a support area II are defined on a semiconductor silicon substrate 40. A p-type  
30 semiconductor silicon substrate 40 is described below for



example. First, a pad layer 41 and a reactive ion etching (RIE) method are employed to pattern a deep trench DT in the substrate 40 within the array area I. Then, a deep trench capacitor 42 including a bottom electrode plate 44, a capacitor dielectric 46 and an upper electrode plate 48 is fabricated at the lower portion of the deep trench DT. Preferably, the bottom electrode plate 44 is an n<sup>+</sup>-type diffusion region, the capacitor dielectric 46 is an ONO (oxide-nitride-oxide) stack structure, and the upper electrode plate 48 is a first polysilicon layer with n<sup>+</sup>-type dopants. Next, in a collar dielectric process, a collar dielectric layer 50 is formed on the sidewall of the deep trench DT. Next, a second polysilicon layer 52 with n<sup>+</sup>-type dopants and a third polysilicon layer 54 are formed in the deep trench DT. Next, a thermal diffusion process is employed to make the n<sup>+</sup>-type dopants diffuse through the third polysilicon layer 54 into the substrate 40, resulting in a buried strap out-diffusion region 56 in the substrate 40 adjacent to the third polysilicon layer 54. Next, deposition and etching are used to form a top isolating layer 58 on the third polysilicon layer 54.

In FIG. 7B, an anti-reflective coating (ARC) layer 60 is formed in the deep trench DT, and a first photoresist layer 62 is patterned on the substrate 40 for defining shallow trench isolations in the array area I and the support area II. Next, using the first photoresist layer 62 as a mask, the exposed portions of the pad layer 41 and the semiconductor silicon substrate 40 are removed to form shallow trenches 63, as shown in FIG. 7C, thus defining an

active area AA within the array area I. Then, the ARC layer 60 and the first photoresist layer 62 are removed.

In FIG. 7D, a nitride liner 64 is conformally deposited on the substrate 40, and then a first HDP (high density plasma) oxide layer 66 is formed to fill the shallow trenches 63. Next, chemical mechanical polishing (CMP) is used to level off the top surfaces of the first HDP oxide layer 66 and the nitride liner 64. Next, in FIG. 7E, a second photoresist layer 68 is provided to cover the support area II. Next, using the nitride liner 64 as an etching stop layer, the first HDP oxide layer 66 within the array area I is removed. Then, the second photoresist layer 68 is removed. In FIG. 7F, after removing the nitride liner 64 and the pad layer 41, a sacrificial oxide layer is formed so as to perform an ion implantation process on the array area I and the support area II for adjusting device threshold voltage.

In FIG. 7G, after removing the sacrificial oxide layer, a thermal oxidation process is employed to grow a gate oxide layer 70 on the exposed silicon surface of the substrate 40. Next, in FIG. 7H, a gate polysilicon layer 72, a metallic silicide layer 74 (such as a WSi layer) and a nitride cap layer 76 are successively deposited on the substrate 40. Then, using a third photoresist layer 78 as a mask to perform an etching process, the gate polysilicon layer 72, the metallic silicide layer 74 and the nitride cap layer 76 within the array area I are patterned as a gate conductive line GC, which partially overlaps two tops of two adjacent deep trenches DT.

In FIG. 7I, after removing the third photoresist layer 78, a second HDP oxide layer 80 is formed to fill the shallow trench 63 outside the active area AA of the array area I, and then CMP is employed to level off the top surfaces of the second HDP oxide layer 80 and the gate conductive line GC. Next, in FIG. 7J, by performing photolithography and etching on the active area AA of the array area I, a first contact hole 82I is formed to penetrate the gate conductive line GC and the gate oxide layer 70, thus exposing the substrate 40.

In FIG. 7K, a nitride spacer 84 is formed on the sidewall of the first contact hole 82I, and then an ion implantation process is performed to form a source/drain diffusion region 86 in the semiconductor silicon substrate 40 exposed by the first contact hole 82I. Next, deposition and CMP for a BPSG layer 88 and deposition and annealing for a TEOS oxide layer 90 are successively performed thereon. Next, using photolithography and etching, a second contact hole 82II is formed to expose the first contact hole 82I and the source/drain diffusion region 86. Finally, in FIG. 7L, the second contact hole 82II is filled with a polysilicon contact layer 92, and then a W/TiN/Ti layer 94 is formed on the polysilicon contact layer 92, and then a bitline 96 is patterned thereon.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore,

Client's ref. :91234

Our ref: 0548-10164-us/final/Cherry/Steve

the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.